REMARKS

Claims 1-24 are pending in the application. Claims 1, 3-9, 11-13, 15-20, and 22-24 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,564,346 to Vollrath *et al.* Claims 1, 2, and 11-14 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,374,378 to Takano *et al.* Claims 1, 2, 13, and 14 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent 6,484,278 to Merritt *et al.* Claims 10 and 21 have been rejected under 35 U.S.C. § 103(a) as being obvious over Takano in view of U.S. Patent No. 6,163,863 to Schicht and U.S. Patent No. 5,418,452 to Pyle, and as obvious over Merritt in view Schicht and Pyle.

Claims 1, 3, 6 and 13 have been amended. Support for the amendments may be found within the entirety of the specification, and particularly at pages 5-8.

I. 35 U.S.C. § 112

The rejection of claim 7 under the 35 U.S.C. § 112, ¶ 2 has been obviated by appropriate amendment.

II. 35 U.S.C. § 102

A. Independent claim 1

Independent claim 1 is directed to a method for configuring a memory apparatus. The method includes sequentially obtaining columns of test information for each of a predetermined number of columns of memory locations within the memory apparatus. The columns of test information are compressed according to associated groups of memory locations to produce a column of compressed test information. Based on the column of

compressed test information, the predetermined number of columns of memory locations may be replaced with a group of redundant memory circuits.

The specification at pages 5-6 describes an exemplary embodiment where test data is obtained for a predetermined number of sets of memory cells. The exemplary embodiment includes comparing columns of data stored in a memory with expected data. The results for each sequential comparison are stored. The stored results are compressed according to associated groups of memory locations to provide a column of compressed data. Applicants respectfully submit that Vollrath, Takano, and Merritt all fail to disclose the limitations of independent claim 1.

Vollrath

First, Vollrath relates to providing a compressed bit fail map. (Vollrath, Abstract). In Vollrath, failure information is transferred to display a compressed bit map by designating areas of the bit map for corresponding failure locations. (Vollrath, Abstract). For each failing cell, the physical address value is generated and translated to a display value where the fail is set at a designated location in the compressed map. (Vollrath, col. 7, ll. 14-16). Row and column maps are generated to identify failures in rows and columns of the memory array. (Vollrath, col. 11, ll. 66-67). The failed rows and columns are replaced after they are identified in the row map and the column map. (Vollrath, col. 12, ll. 1-2). The row map and column map may be compressed to generate a subarray so that memory cell failures can also be replaced. (Vollrath, col. 11, ll. 66-67). Vollrath merely discloses that the map may be compressed by an operation "that may include an algorithm, a Boolean operation, a lookup

table, or hardware switch array to convert addresses to display addresses in a plurality of compressed bit maps." (Vollrath, col. 12, ll. 6-21). Accordingly, Vollrath discloses merely that a map space is compressed to display addresses in a plurality of compressed bit maps.

Applicants submit that Vollrath does not disclose configuring a memory apparatus as recited in claim 1. In particular, Vollrath does not disclose sequentially obtaining columns of test information for each of a predetermined number of columns of memory locations. Vollrath also does not compress columns of test information "according to associated groups of memory locations to produce a column of compressed test information." Figures 1B-1E show magnified views of mapped failures indicated by labels 1B-1E in Figure 1A. (Vollrath, col. 4, ll. 23-26). However, Figures 1B-1E do not illustrate "sequentially obtaining columns of test information" as recited by claim 1, or to compress columns of test information "according to associated groups of memory locations to produce a column of compressed test information. Accordingly, Vollrath does not disclose each limitation of claim 1.

Takano

Next, Takano relates to failure analysis where comparisons of output data of a memory with expected data are input as fail data to fail data compressing/bit positions. (Takano, Abstract). In Takano, data are compressed into the data-width direction into one-bit data displaced apart in the bit position. (Takano, Abstract). That is, Takano illustrates a plurality of fail data compression/bit position setting means 20A through 20D that are each identical in construction. (Figures 4 and 7; col. 5, ll. 25-30). Each fail data compression/bit position setting means 20A through 20D compresses fail data, sets the bit position of

compressed fail data CFL0 to CFL3 of an arbitrary bit position and outputs the data as "noncompressed data." (Figures 4 and 7; col. 5, ll. 30-40). The fail data compression/bit position setting means 20A through 20D are allowed to use a memory part 16C singly and hence "store the fail data intact without compressing it." (col. 5, l. 65 to col. 6, l. 1). Accordingly, Takano discloses merely to store failure data. (see col. 4, ll. 50-56).

Applicants submit that the failure analysis of Takano does not replace a predetermined number of columns of memory locations with a group of redundant memory circuits, "based on the column of compressed test information." Indeed, in Takano, fail data are store[d] in a memory "intact without compressing it." Furthermore, Takano does not sequentially obtain columns of test information for each of a predetermined number of columns of memory locations or compress columns of test information "according to associated groups of memory locations to produce a column of compressed test information." Accordingly, Takano does not disclose the limitations of claim 1.

Merritt

Merritt relates to a test circuit that tests for defective memory cells of an Embedded DRAM. (Merritt, Abstract). In Merritt, a storage circuit latches error signals to sequentially transfer latched errors onto a terminal of the DRAM. (Merritt, Abstract). Merritt discloses a control circuit that utilizes compression circuitry to write test data placed on a single terminal of the DRAM into a plurality of memory cells in the memory under test. (col. 7, ll. 1-4).

Applicants submit that Merritt does not disclose any method for configuring a memory apparatus, as recited in claim 1. In particular, Merritt does not disclose sequentially

obtaining columns of test information for each of a predetermined number of columns of memory locations. Merritt also does not compress columns of test information "according to associated groups of memory locations to produce a column of compressed test information." Accordingly, Merritt does not each limitation of claim 1 and therefore, Applicants submit that independent claim 1 is not anticipated by Merritt. Applicants respectfully request reconsideration of the pending rejections of claim 1.

B. Independent claim 13

Independent claim 13 is directed to an apparatus for configuring a memory. The apparatus includes an input for sequentially receiving columns of test information for each of a predetermined number of columns of memory locations. The apparatus also includes a compression apparatus that compresses the columns of test information according to associated groups of memory locations to produce a column of compressed test information. A replacement apparatus is operable based on the compressed test information to replace a group of redundant memory circuits respectively associated with the predetermined number of columns of memory locations.

Applicants submit that Vollrath, Takano and Merritt do not disclose the limitations of independent claim 13. First, as discussed, Vollrath relates to providing a compressed bit fail map in which failure information is transferred to display a compressed bit map by designating areas of the bit map for corresponding failure locations. (Vollrath, Abstract). However, Vollrath does not sequentially obtain columns of test information for each of a predetermined number of columns of memory locations or compress columns of test information "according to associated groups of memory locations to produce a column of

compressed test information." Accordingly, Vollrath does not disclose the limitations of claim 13

Next, as discussed with regard to Takano, Takano does not replace a predetermined number of columns of memory locations with a group of redundant memory circuits, "based on the column of compressed test information," sequentially obtain columns of test information for each of a predetermined number of columns of memory locations, or compress columns of test information "according to associated groups of memory locations to produce a column of compressed test information." Accordingly, Takano does not disclose the limitations of claim 13.

Finally, regarding Merritt, Applicants submit that the Merritt does not sequentially obtain columns of test information for each of a predetermined number of columns of memory locations, or compress columns of test information "according to associated groups of memory locations to produce a column of compressed test information." Accordingly, Merritt does not each limitation of claim 13 and therefore, Applicants submit that independent claim 13 is not anticipated by Merritt. Applicants respectfully request reconsideration of the pending rejections of claim 13.

Dependent Claims

For similar reasons, Vollrath, Takano and Merritt also fail to disclose the limitations of claims 2-12 and 14-24. As discussed above, Vollrath, Takano and Merritt do not disclose the limitations for independent claims 1 and 13, and therefore, Vollrath, Takano and Merritt also do not disclose the limitations for claims dependent therefrom. Accordingly, Applicants also respectfully request favorable consideration of claims 2-12 and 14-24.

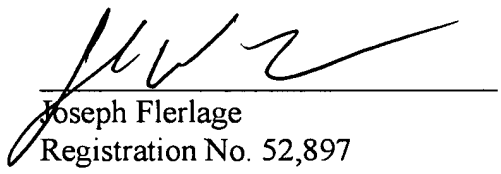
III. 35 U.S.C. § 103

Claims 10 and 21 have been rejected as being obvious over Takano in view Schicht and Pyle as well as Merritt *et al.* in view Schicht and Pyle. As discussed, Applicants respectfully submit that neither Takano nor Merritt disclose or suggest the limitations of independent claims 1 and 13. Therefore, the inventions of claims 10 and 21, which depend from claims 1 and 13 respectively, would not be obvious over Takano or Merritt in combination with the Schicht, and Pyle. Accordingly, Applicants respectfully submit that the Takano, Schicht, and Pyle combination and the Merritt, Schicht, and Pyle combination do not disclose or suggest the limitations of claims 10 and 21.

CONCLUSION

In view of the foregoing amendments and reasons, Applicant respectfully requests favorable consideration and earnestly solicits allowance of all pending claims. Inquiries regarding this communication may be directed to the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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